Fig. 1a

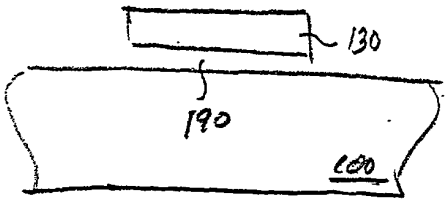


Fig. 1b

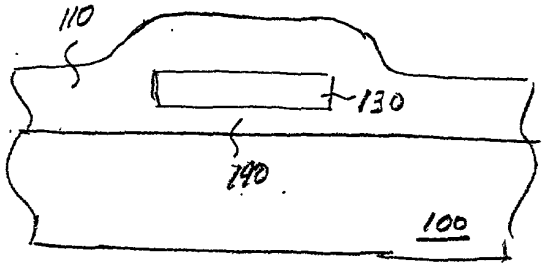


Fig. 1c

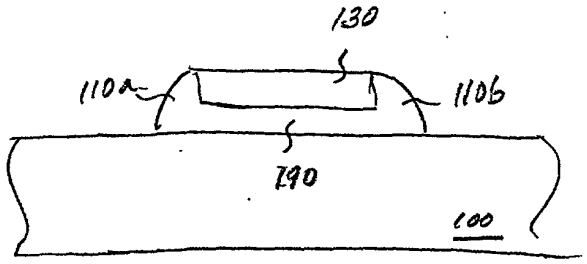
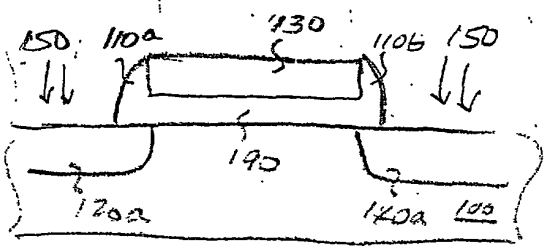


Fig. 1d



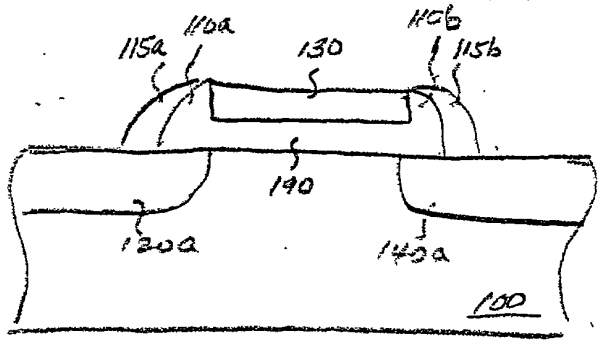


Fig. 1e

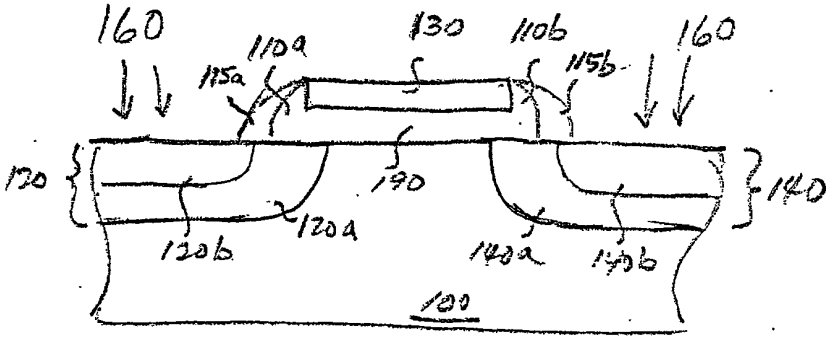


Fig. 1f

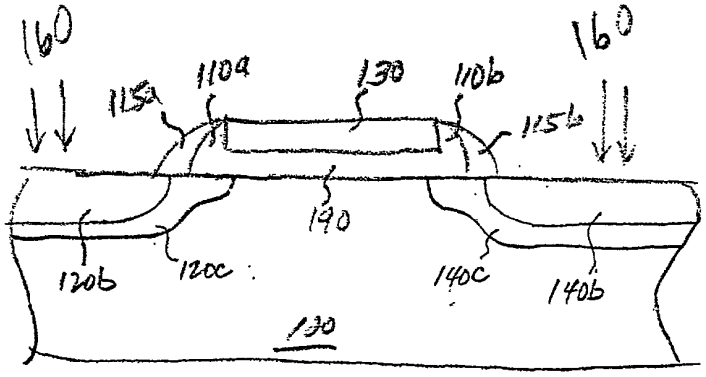


Fig. 1g

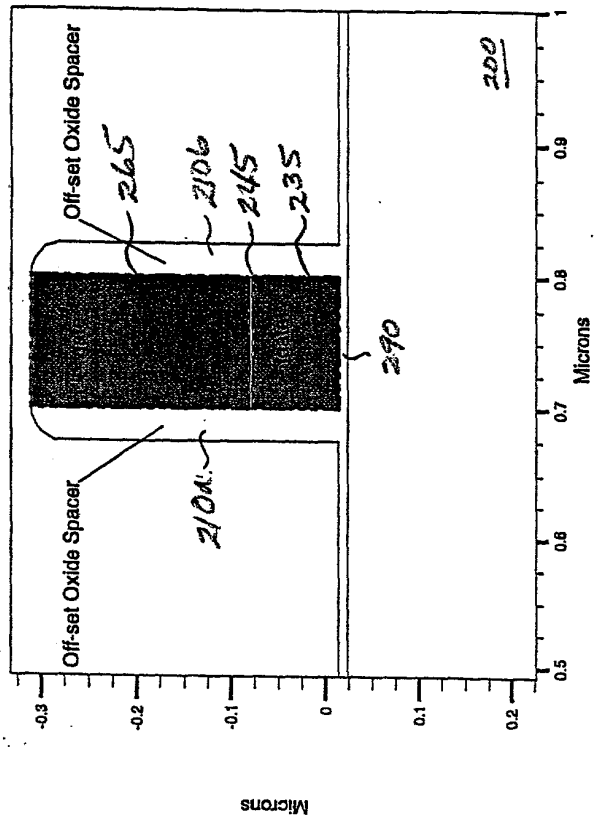


Fig. 2b

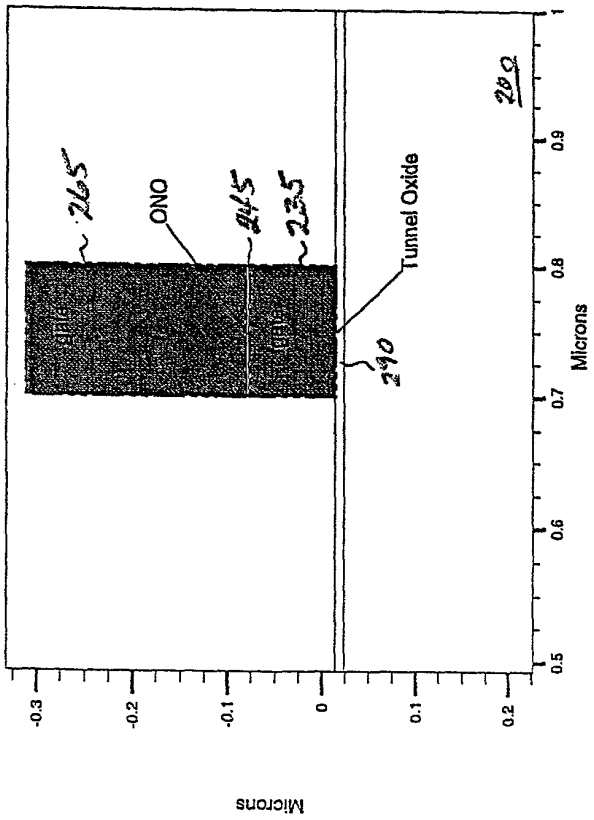


Fig. 2a

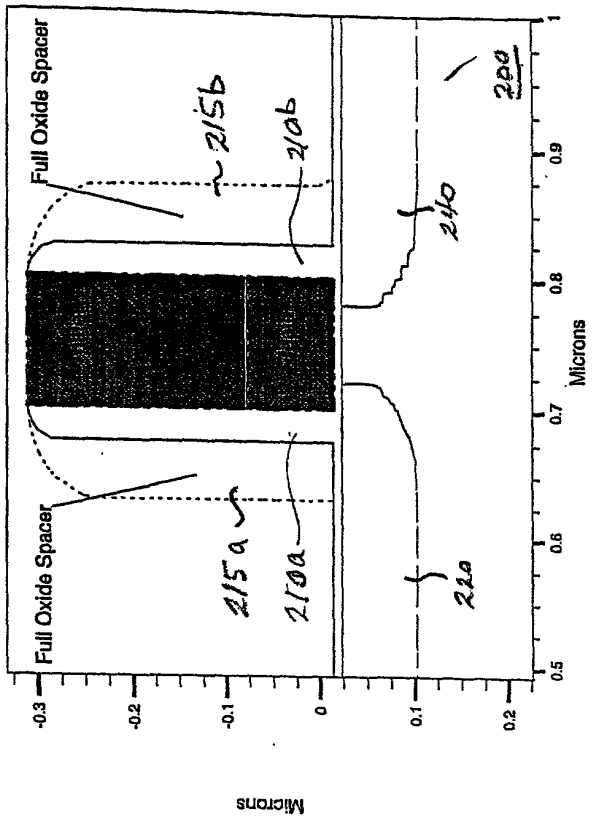


Fig. 2d

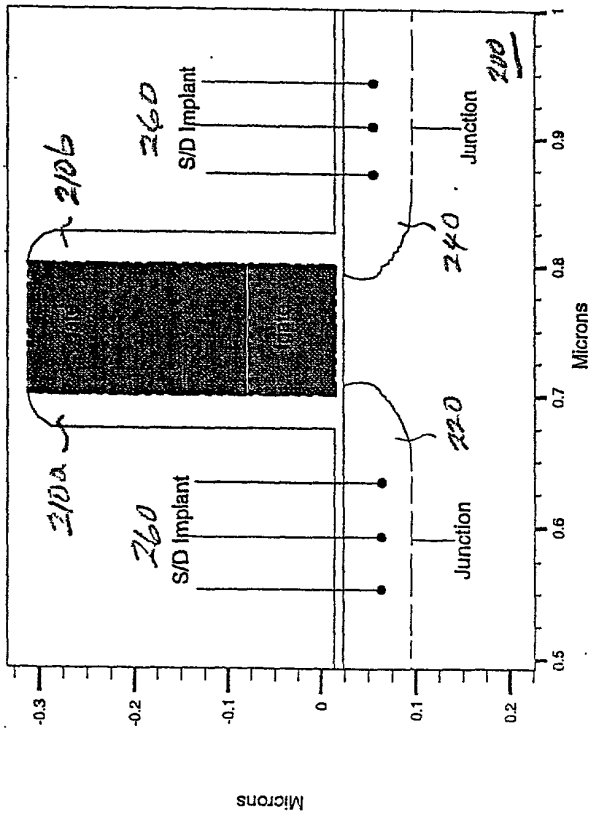


Fig. 2c

Array Cell

Periphery DDD HV transistor

Periphery LDD LV transistor

Fig. 3a

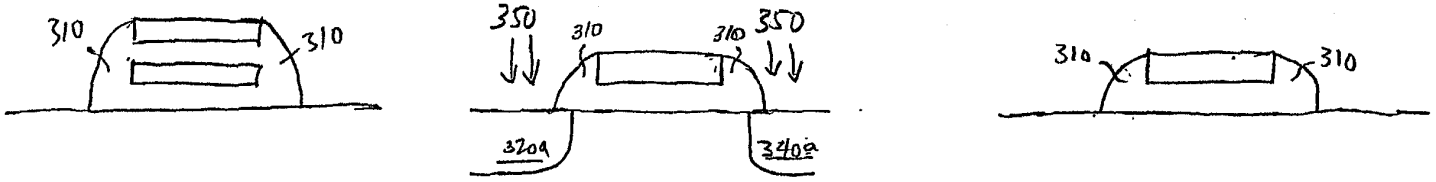


Fig. 3b

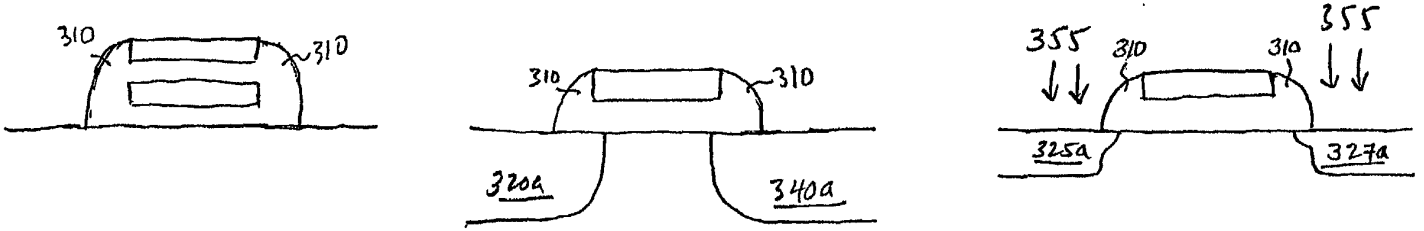


Fig. 3c

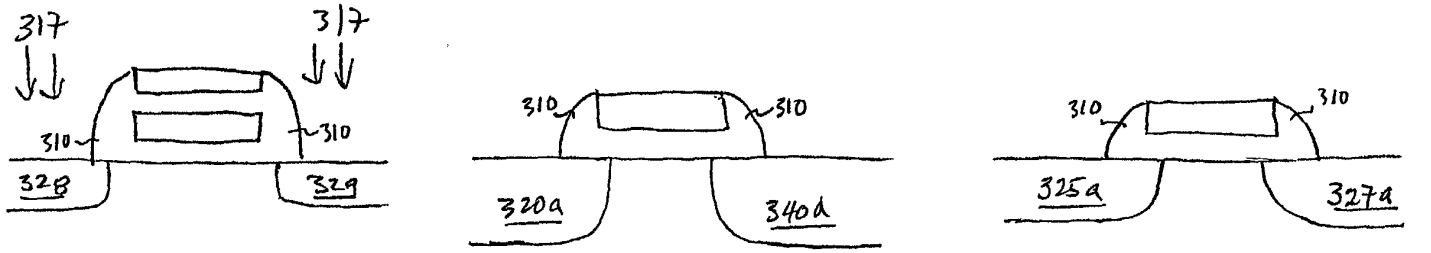


Fig. 3d

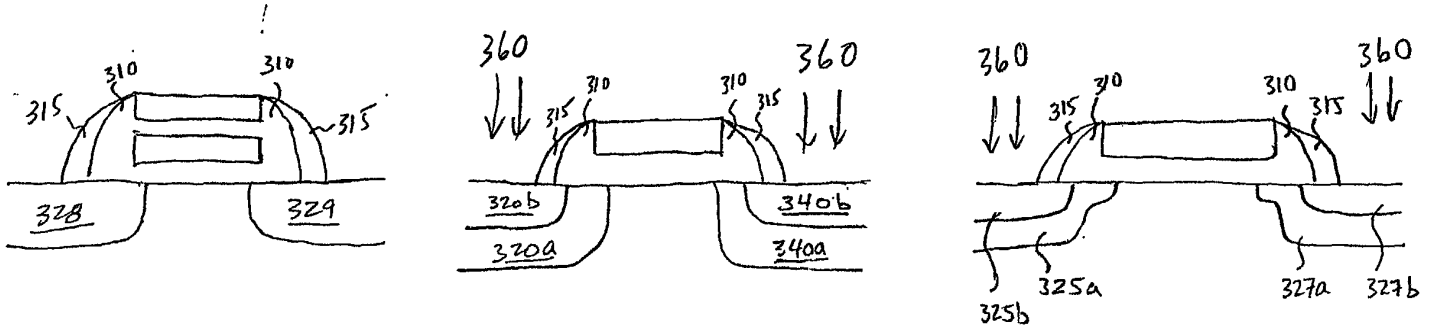


Fig. 4a

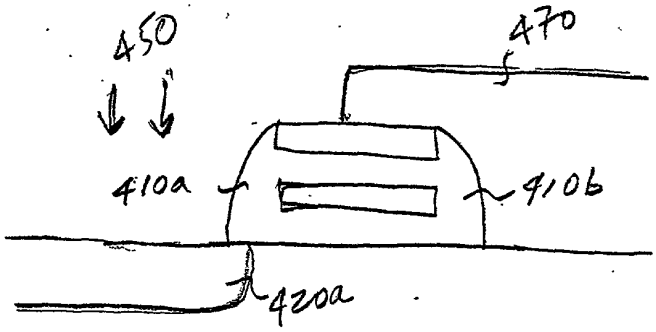


Fig. 4b

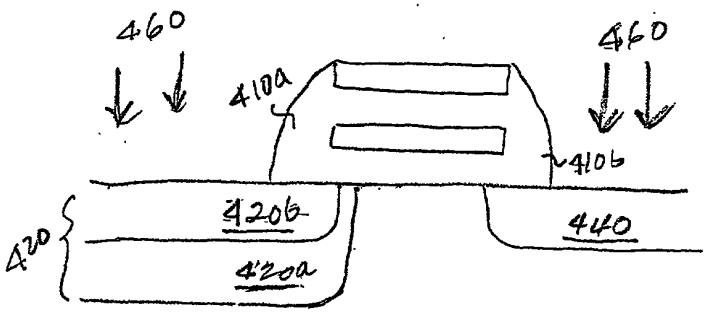


Fig. 5a

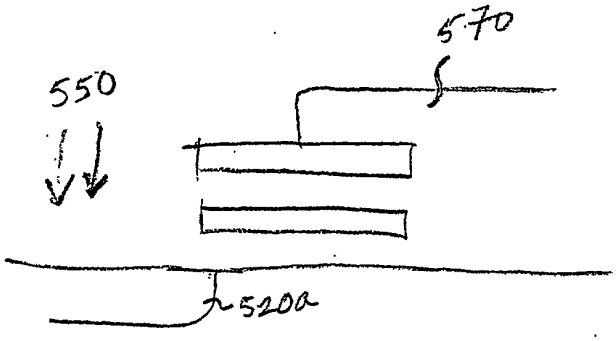
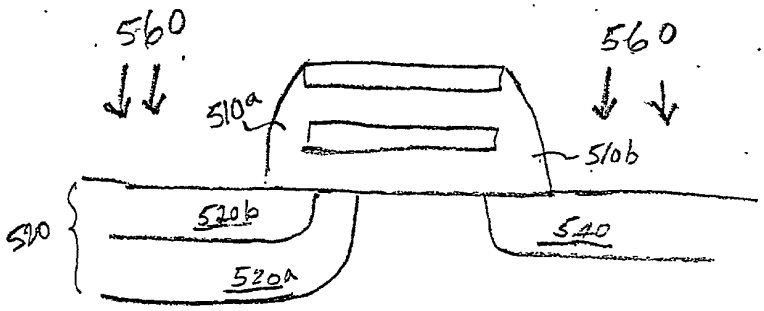


Fig. 5b



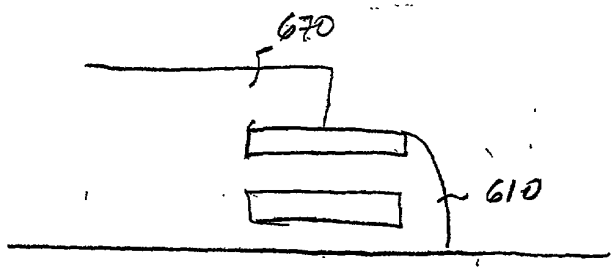


Fig. 6

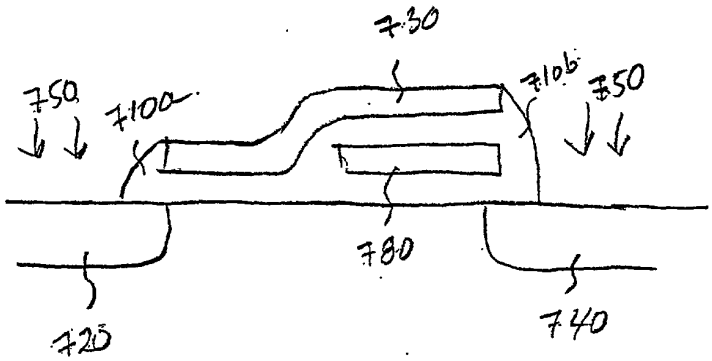


Fig. 7